UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/266,869	03/12/99	TANIGUCHI K	P8075-9008

TM01/0620
ARENT FOX KINTNER PLOTKIN & KAHN PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 600
WASHINGTON, DC 20036-5339

EXAMINER	
PATEL, G	
ART UNIT	**PAPER NUMBER**
2183	4

DATE MAILED: 06/20/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/266,869	03/12/99	TANIGUCHI K	P8075-9008

EXAMINER	
PATEL, G	
ART UNIT	**PAPER NUMBER**
2183	

TM02/0329
NIKAIDO MARMELSTEIN MURRAY & ORAM
METROPOLITAN SQUARE
655 FIFTEENTH STREET NW
SUITE 330 G STREET LOBBY
WASHINGTON DC 20005-5701

DATE MAILED: 03/29/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/266,869	Taniguchi et al.
Examiner	**Group Art Unit**
Gautam R. Patel	2183

☒ Responsive to communication(s) filed on *Mar 12, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-18* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-16* is/are rejected.

☒ Claim(s) *17 and 18* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-18 are pending for the examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119, which papers have been placed of record in the file.

Specification

3. The disclosure is objected for following reasons.

The title of the invention is neither precise nor descriptive. A new title is required which should include, using twenty words or fewer, claimed features that differentiate the invention from the Prior Art.

Correction is required.

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly

owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

5. Claims 1-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants admitted prior art (AAPA) (specification page 1-2) in view of Hoskins, US. patent 5,872,978 (hereafter Hoskins).

As to claim 1, AAPA Hoskins discloses the invention as claimed [see Figs. 1], including reading program from memory and detecting pseudo instruction comprising: a method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, at least one instruction address of or data address being part of the pseudo instruction [see spec. Page 1, line 22 to page. 2, line, 7] the method comprising the steps of:

a. reading the program from the memory [spec. Page 1, line 22 to page. 2, line, 7];

b. prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address; and

storing the prefetched instruction or data in a buffer [spec. Page 1, line 22 to page. 2, line, 7].

regarding claim 1 , AAPA teaches prefetching of instruction or data from a memory AAPA also teaches detecting a branch instruction prior to execution of the branch instruction. AAPA proposes a hardware solution for the detection of branch. Hoskins proposes a software solution for detecting a branch. One skilled in the art would have clearly recognized that the software reduces the cost of extra hardware necessary to implement the detection scheme. One of ordinary skill in the art at the

time of invention would have been motivated to implement Hoskins' branch detection scheme with the help of the pseudo-instruction [col. 2, lines 4-21] in the system of AAPA, because it would have reduced the cost of system implementation.

6. As to claim 2, Hoskins discloses:

providing a pseudo instruction detection unit [fig. 1, unit 24] connected with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit with the buffer.

Hoskins does not teach that the buffer and detection units are connected in parallel. However it would have been obvious to a person of ordinary skill at the time of the invention to have placed the buffer and detection unit in parallel and put them into the system of AAPA and Hoskins because doing so would make design more faster. As shown in "In re Japikse **86 USPQ 70 (CCPA 1950)**", to rearrange parts for different storage method is generally not given patentable weight or would have been obvious improvements.

7. As to claim 3:

. the buffer includes first and second buffers connected in parallel with the memory, and the method further comprising a step of storing, the instruction and data read from the memory in the first buffer and storing the prefetched instruction or data in the second buffer;

Hoskins does not teach additional instruction memories or plurality of additional data memories. However it would have been obvious to a person of ordinary skill at the time of the invention to have combined additional instruction memories and additional data memories and put them into the system of AAPA and Hoskins because doing so would make design more faster by storing these instructions and data in additional buffers. As shown in "St. Regis Paper Co. v Bemis Co. **193 USPQ 8 (7th Cir. 1977)**", to

duplicate parts for multiple effects is generally not given patentable weight or would have been obvious improvements.

8. As to claim 4, Hoskins discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer when the pseudo instruction is detected [col. 2, lines 4-20];

as to rest of the claim AAPA discloses:

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address after the transfer of the at least one instruction to the first buffer has been identified [spec. Page 1, line 22 to page. 2, line, 7].

9. As to claim 5, Hoskins discloses:

Identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected [col. 2, lines 4-20];

as to rest of the claim AAPA discloses:

wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer [spec. Page 1, line 22 to page. 2, line, 7].

10. As to claim 6, it is rejected for the same reasons set forth in the rejection of claim 4, supra.

11. As to claim 7, it is rejected for the same reasons set forth in the rejection of claim 5, supra.

12. As to claim 8, Hoskins discloses:

a buffer [fig. 1, unit 22], connected to a memory [fig. 1, unit 12], for storing instructions and data of a program prefetched from the memory, wherein the program

includes a pseudo instruction, at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, and at least one instruction address or data address being part of the pseudo instruction [col. 3, lines 25-40 and col. 4, lines 4-43] ;

an instruction execution unit [fig. 1, unit 26 and fig. 2, step 110], connected to the buffer [fig. 1, unit 22], for receiving the instruction and data from the buffer and executing a predetermined processing operation using the instruction and data [col. 3, lines 25-40 and col. 4, lines 4-43];

a pseudo instruction detection unit [fig. 1, unit 24], connected to the memory, for detecting the pseudo instruction included in the program prefetched from the memory; and the pseudo instruction detection unit [col. 3, lines 25-40 and col. 4, lines 4-43];

as to the rest of the claim 8 AAPA discloses:

an address control unit, prefetching the instruction or data in accordance with at least one instruction address or data address when the pseudo instruction is detected H [spec. Page 1, line 22 to page. 2, line, 7].

13. As to claim 9, it is rejected for the same reasons set forth in the rejection of claim 3, supra.

14. As to claim 10, Hoskins discloses:

the address control unit identifies that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected and permits storage of the instruction or data in the second buffer when the corresponding instruction or data is not stored in the second buffer [col. 2, line 65 to col. 3, line 21 and col. 8, lines 5-39].

15. As to claim 11, it is rejected for the same reasons set forth in the rejection of claim 2, supra.

16. As to claim 12, it is rejected for the same reasons set forth in the rejection of claim 10, supra.

17. As to claim 13, it is rejected for the same reasons set forth in the rejection of claim 11, supra.

18. As to claim 14, Hoskins discloses:

a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction [col. 3, lines 25-40 and col. 4, lines 4-43]; as to the rest of the claim

combination of AAPA and Hoskins does not disclose a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for validating the opcode detection operation during an operand transfer period. "Official Notice" is taken that both the concept and the advantages of providing a detection timing circuit which can calculate transfer period based on the instruction length and number of operands are well known. It would have been obvious to provide a timing circuit to AAPA and Hoskins' system as this circuit is known to provide the system with a timing estimate and send valid operand into the system. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

19. As to claim 15, it is rejected for the same reasons set forth in the rejection of claim 1, supra.

As to added limitation of the recording medium having program stored in them [see fig. 1, unit 12, Hoskins].

20. As to claim 16, it is rejected for the same reasons set forth in the rejection of claim 1 and 8, supra.
As to the added limitation of
a bus interconnecting the prefetch buffer and the memory [inherently present].

Allowable Subject Matter

21. Claims 17 and 18 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

NOTES & REMARKS

It is not clear from the abstract of prior art [IDS ref. 1] that how pseudo-instruction is related to the scheme of branch detection. Explanation from the Applicants will be appreciated.

Other prior art cited

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
    a. Matsuo et al. (US. patent 4,858,104) "Preceding instruction address based branch prediction in a pipelined processor".
    b. Grochowski et al. (US. patent 5,442,756) "Branch prediction and resolution apparatus for a superscalar computer processor".

c. Weiser et al. (US. patent 5,265,213) "Pipelined system for executing predicted branch target instruction in a cycle concurrently with execution of branch instruction".

d. Puzak et al. (US. patent 5,790,823) "Operand prefetch table".

Contact information

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie P. Chan, can be reached on (703) 305-9712. The fax phone number for this Group is (703) 306-5404.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-3900.

GRP

Gautam R. Patel
Patent Examiner
Group Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

March 24,2001